AMENDMENTS TO THE CLAIMS

Please cancel claim 4, amend claim 1 and add new clams 5-9 as follows:

1. (Currently Amended) A method of manufacturing a flash memory device, comprising ~~the steps of~~:

performing an ion implantation for controlling a threshold voltage on a semiconductor substrate;

performing a spike annealing for controlling a doping concentration and a doping profile of an implanted dopant, wherein the spike annealing is performed under NH_3, H_2, or N_2 atmosphere at a temperature in the range of 900°C to 1,100°C with a heating rate of 100°C/sec to 250°C /sec;

forming a device isolation film for isolating an active area and a field area on the semiconductor substrate;

forming a gate electrode in which a tunnel oxide film, a floating gate electrode, a dielectric film, and a control gate electrode are deposited on the active area; and

performing an ion implantation for forming junctions on the semiconductor substrate in both sides of the gate electrode to form a DDD junction structure.

2. (Original) The method of manufacturing a flash memory device according to claim 1, wherein the ion implantation for controlling a threshold voltage is performed by using a p-type dopant with an ion implantation energy of 5 KeV to 50 KeV and a dose of 1E11 ion/cm^2 to 1E13 ion/cm^2.

3. (Original) The method of manufacturing a flash memory device according to claim 2, wherein BF_2 is used as the p-type dopant.

4. (Cancelled)

5. (New) A method of manufacturing a flash memory device, comprising:

performing an ion implantation for controlling a threshold voltage on a semiconductor substrate;

performing a spike annealing for controlling a doping concentration and a doping profile of an implanted dopant, wherein the spike annealing is performed under NH_3, H_2, or N_2 atmosphere;

forming a device isolation film for isolating an active area and a field area on the semiconductor substrate;

forming a gate electrode in which a tunnel oxide film, a floating gate electrode, a dielectric film, and a control gate electrode are deposited on the active area; and

performing an ion implantation for forming junctions on the semiconductor substrate in both sides of the gate electrode to form a DDD junction structure.

6. (New) The method of manufacturing a flash memory device according to claim 1, wherein the ion implantation for controlling a threshold voltage is performed by using a p-type dopant with an ion implantation energy of 5 KeV to 50 KeV and a dose of 1E11 ion/cm^2 to 1E13 ion/cm^2.

7. (New) The method of manufacturing a flash memory device according to claim 6, wherein BF_2 is used as the p-type dopant.

8. (New) The method of manufacturing a flash memory device according to claim 6 wherein the spike anneal is carried out at a temperature in the range of 900°C to 1,100°C with a heating rate of 100°C/sec to 250°C /sec.

9. (New) The method of manufacturing a flash memory device according to claim 7 wherein the spike anneal is carried out at a temperature in the range of 900°C to 1,100°C with a heating rate of 100°C/sec to 250°C /sec.

10. (New) The method of manufacturing a flash memory device according to claim 6 wherein the spike anneal is carried out at a temperature in the range of 900°C to 1,100°C with a heating rate of 100°C/sec to 250°C /sec.